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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,363	07/12/2000	John M. Airey	2839/115	2211

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EXAMINER	
WANG, JIN CHENG	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
02/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/614,363	AIREY ET AL.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-13,22,26-33,35-37,45,47-56,58-60,62 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 5-13, 22, 26-33, 35-37, 45, 47-56, 58-60, and 62-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendments

Applicant's submissions filed on 1/11/2008 have been entered. Claims 2, 4, 14-21, 23-25, 34, 38-44, 46, 57 and 61 have been canceled. Claims 1, 3, 5-13, 22, 26-33, 35-37, 45, 47-56, 58-60, and 62-63 are pending in the application.

Response to Arguments

Applicant's arguments filed January11, 2008 have been fully considered. Applicant filed a terminal disclaimer on 1/11/2008 and therefore the obvious-type double patenting rejection in the prior Office Action dated 7/13/2007 is withdrawn.

Applicant argues with respect to the claim 31 and similar claims that the Baum reference has a common assignee at the time the claimed invention was filed. The examiner thus withdraw the 103 rejection based on Baum. However, the claim invention is fulfilled by Baum for the reasons given in the present Office Action based on further consideration of the Baum reference in view of the claimed invention.

As addressed below, Baum teaches a processor for performing geometric calculations on a plurality of vertices of a primitive (Fig. 6 and column 16, lines 17-67);

A rasterization circuit coupled to the processor that rasterizes the primitive according to a scan conversion process which operates using a floating point format (*Fig. 6, column 9, lines 50-65 the polygons, triangles and vertices are rasterized on per-vertex basis and interpolated inside the triangle. The polygons, triangles and vertices are converted to pixels in the rasterization using the technique of interpolation. Rasterization includes the step of scan conversion in which*

the geometric objects are scan converted to pixels in the raster order, i.e., the polygons, triangles and/or vertices are scan converted to the pixels in the raster order; see column 16, lines 17-67 and column 17, lines 20-50; Baum teaches in Fig. 6, column 9, lines 50-65 and column 16, lines 17-67 the triangle rasterization, which is also referred to as triangle scan-conversion, is typically performed by an algorithm consisting of an interpolation phase----see column 17, lines 20-50. The triangle rasterization is based on an algebraic representation of the triangle by vertices and vectors. The current rasterization position in the screen space involves the computation of the cross-product---see column 17, lines 20-50. This cross-product can be expressed for any arbitrary pixel position on the screen as an analytical function. The pixel color values depend upon the result of an evaluation at the current rasterization position. As the triangle is scanned, all primitives/fragments are interpolated],

A frame buffer coupled to the rasterization circuit for storing a plurality of color values in floating point formats (*Floating point frame buffer is explicitly taught in column 12, lines 58-64; see also Fig. 6; see column 10, lines 40-65 and column 11, lines 1-40 wherein color values are calculated as floating point values; see column 13, lines 27-55 wherein the red, green and blue components of each pixel are equal to the respective x, y and z components of the irradiance vector at that point. Because the irradiance vector is calculated as a floating point vector---see column 10, lines 40-65 and column 11, lines 1-40. The color values in the frame buffer are floating point values*).

Therefore, the claimed invention is fulfilled by Baum for the reasons given above.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5-13, 22, 26-33, 35-37, 45, 47-56, 58-60, and 62-63 are rejected under 35 U.S.C. 102(e) as being anticipated by Baum et al U.S. Patent No. 6,567,083 (hereinafter Baum).

Re claims 1, 31 and 45, Baum teaches a processor for performing geometric calculations on a plurality of vertices of a primitive (Fig. 6 and column 16, lines 17-67);

A rasterization circuit coupled to the processor that rasterizes the primitive according to a scan conversion process which operates using a floating point format (*Fig. 6, column 9, lines 50-65 the polygons, triangles and vertices are rasterized on per-vertex basis and interpolated inside the triangle. The polygons, triangles and vertices are converted to pixels in the rasterization using the technique of interpolation. Rasterization includes the step of scan conversion in which the geometric objects are scan converted to pixels in the raster order, i.e., the polygons, triangles and/or vertices are scan converted to the pixels in the raster order; see column 16, lines 17-67 and column 17, lines 20-50; Baum teaches in Fig. 6, column 9, lines 50-65 and column 16, lines 17-67 the triangle rasterization, which is also referred to as triangle scan-conversion, is typically performed by an algorithm consisting of an interpolation phase----see column 17, lines 20-50. The triangle rasterization is based on an algebraic representation of the triangle by vertices and vectors. The current rasterization position in the screen space involves the computation of the cross-product---see column 17, lines 20-50. This cross-product can be*

expressed for any arbitrary pixel position on the screen as an analytical function. The pixel color values depend upon the result of an evaluation at the current rasterization position. As the triangle is scanned, all primitives/fragments are interpolated),

A frame buffer coupled to the rasterization circuit for storing a plurality of color values in floating point formats (*Floating point frame buffer is explicitly taught in column 12, lines 58-64; see also Fig. 6; see column 10, lines 40-65 and column 11, lines 1-40 wherein color values are calculated as floating point values; see column 13, lines 27-55 wherein the red, green and blue components of each pixel are equal to the respective x, y and z components of the irradiance vector at that point. Because the irradiance vector is calculated as a floating point vector---see column 10, lines 40-65 and column 11, lines 1-40. The color values in the frame buffer are floating point values*).

Re claims 3 and 47, Baum discloses a texture circuit coupled to the rasterization circuit with the graphics pipeline that applies a texture to the primitive, wherein the texture is specified by floating point values and a texture memory coupled to the texture circuit that stores a plurality of textures in floating point values (See Fig. 6 and column 14).

Re claims 5 and 48, Baum discloses the floating-point format is comprised of sixteen bits (column 10-11; see column 7, lines 10-30 wherein the floating point values require the floating point in sixteen bits and the double represents the thirty-two-bits values).

Baum discloses floating-point values have 16 bits (column 10-11; see column 7, lines 10-30 wherein the floating point values require the floating point in sixteen bits and the double represents the thirty-two-bits values)

Re claims 7 and 50, Baum discloses a lighting circuit coupled to the rasterization circuit for performing a lighting function, wherein the lighting function executes on floating point values (**Fig. 16 and column 14**).

Re claims 6, 8-13 and 22, 49, and 51-56, 58-60 and 62-63, the limitations of claims 6, 8-13, 22, 49 and 51-56, 58-60 and 62-63 are analyzed as discussed with respect to claim 1.

Re claim 26, Baum discloses the steps of writing, storing, and reading the data in the frame buffer in the floating point format are further comprised of specifying the floating-point format according to a specification, wherein the specification corresponds to a level of range and precision (**Fig. 6 and column 10-16**).

Re claims 32-33 and 35, Baum discloses the floating point color values are written to, read from (for display purposes), and stored in the frame buffer (**column 13, lines 25-65**).

Re claims 36-37, Baum discloses the floating point color values are comprised of 16 bits of data and the data are comprised of one sign bit, ten mantissa bits, and five exponent bits (column 10-16; column 10-11; see column 7, lines 10-30 wherein the floating point values require the floating point in sixteen bits and the double represents the thirty-two-bits values).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jcw Jianchong Wang, P.E.